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10/752,131	01/06/2004	Hae-Seung Lee	7033C	3915

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EXAMINER	
HSU, AMY R	

ART UNIT	PAPER NUMBER
2609	

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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/752,131	LEE ET AL.	
	Examiner	Art Unit	
	Amy Hsu	2609	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *06 January 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-21* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-21* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *06 January 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date *2/13/2006 and 9/7/2004*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

Claim Rejections - 35 USC § 112

1. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

2. Claim 1 is rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Regarding Claim 1, the term "integration period" is defined in applicant's specification as the period, immediately following the soft reset until the initiation of the next reset (*Paragraph 43).* Claim 1 claims a first reset pulse, or the first reset, at the beginning of an integration period, which would make the first reset pulse occur immediately following the soft reset when applying the applicant's definition of integration period. The soft reset mentioned in the applicant's definition of integration period is the first reset, so the first reset cannot take place after the first reset. Applicant's specification supports the first reset (*Fig. 3 reference A to C)* is followed by the integration period (*Fig. 3 reference E to F is the integration period)* which is followed by a second reset (*Fig. 3 reference G to J*). It is indefinite how the reset pulse occurs at the beginning of the integration period as stated in Claim 1 because the specification only supports the integration period happening at the end of the first reset. For purposes of prosecution, the examiner will use what is clearly taught in applicant's

specification that the first reset pulse is followed by the integration period followed by the second reset pulse.

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. Claims 1-6 are rejected under 35 U.S.C. 103(a) as being unpatentable over Bencuya et al. (US 6911640) in view of Watanabe (US 6163023).

Regarding Claim 1, Bencuya teaches a circuit for a pixel site in an imaging array, comprising (*Fig. 1 and Col 3 Lines 17-19)*: a pixel to convert incident light to an electrical signal (*Col 3 Line 18 describes pixel which comprises a photodiode to convert light to electrical signal as described in Col 3 Lines 42-45)*; a row line to read out a voltage from said pixel (*Fig. 1 reference number 124 connects to a column bus, which connects to reference number 110, the read select transistor, and Col 3 Lines 31-35, see also note on next paragraph regarding column bus and row line)*; a row line transistor (*Fig. 1 reference number 106)*, operatively connected between one end of said row line (*Fig. 1 reference number 118 connected to 110)* and a predetermined voltage, to reset a voltage associated with said row line (*Fig. 1 reference number 118 connected to 114, which sets a potential as described in Col 5 Lines 58-61 to reset*

106, the row line transistor, or reset transistor); and a reset voltage generator, operatively connected to said row line transistor, to generate reset pulses (*Fig. 1 reference number 114 is the circuitry to generate reset voltage and is connected to 106 to generate a reset pulse as described in Col 5 Lines 66-67 through Col 6 Lines 1-3 and pictured in Fig. 5)*; Bencuya teaches the rest voltage generator generating a reset pulse (*Fig. 3A)* but is silent on more options after the first reset pulse.

Note: A row is defined as a number of things arranged in a line, especially a straight line. Therefore a column is a row, and the column bus referred to in Bencuya teaches the row line of the present application. Fig. 1 of Bencuya teaches reference number 124 which connects to a column bus which is the row line, and reference number 106 is the row line transistor.

Watanabe teaches similar circuitry for a pixel site of an imaging array in Fig. 1A with a voltage generator, or supply, used for reset transistor (*Fig. 1A reference number 14 applied to reference number 2, the reset transistor) to generate* a first reset pulse (*Fig. 1B Step S101)*; and generates a second reset pulse after generating said first reset pulse, the generation of the second reset pulse being at an end of the integration period of said pixel (*Fig. 1B Step 105, which happens after the integration period)*. Note: Integration time is the time between Steps S101 and S105.

It would have been obvious to one of ordinary skill in the art at the time of the invention to modify the teachings of Bencuya which teaches a reset pulse by adding a second reset pulse after a period of time because the pulses are repeated since the

circuitry described corresponds to a pixel site, the pulses have to be repeated to go through all the pixel sites.

Regarding Claim 2, Bencuya in view of Watanabe teach the circuit as claimed in claim 1, Bencuya also teaches said pixel comprising (*Col 3 Lines 17-18 describes the pixels each comprise the following)*: a light-detecting element to convert incident light to a photocurrent (*Fig. 1 reference number 104 and Col 3 Lines 42-45*); a reset transistor (*Fig. 1 reference number 106*), operatively connected to said light-detecting element (*Fig. 1 reference number 106 is connected to 104 by node 120)*, to reset a voltage associated with said light-detecting element (*Col 3 Lines 54-56*); and a pixel reset voltage generator (*Fig. 1 reference number 114)*, operatively connected to a non-gate terminal of said reset transistor (*connected at node 118 to non-gate terminal or reset transistor)*, to generate a reset voltage (*Col 7 Lines 53-55)*; said pixel reset voltage generator generating a first pixel reset voltage; said pixel reset voltage generator generating a second pixel reset voltage after generating said first pixel reset voltage (*as addressed in the paragraph addressing Claim 1 where the pixel reset voltage generated by the reset voltage generator, reference number 114, is the same as the reset pulse generated by reference number 114 in Claim 1*).

Regarding Claim 3, Bencuya in view of Watanabe teach the circuit as claimed in claim 1, wherein said predetermined voltage is ground. Bencuya teaches V_g as the voltage level generated by reset gate voltage circuitry (*Col 7 Lines 55-57).* This is a

predetermined voltage because it is determined before the reset operation. Bencuya teaches this predetermined voltage is ground (*Col 8 Lines 32-33).*

Regarding Claims 4 and 5, Bencuya in view of Watanabe teach the circuit as claimed in claim 2, Bencuya also teaches said pixel further comprising: a transistor (*Fig. 1 reference number 108*); said transistor having a gate thereof operatively connected to said light-detecting element (*the gate of 108 is connected to 104 through node 120)*; said transistor having a non-gate terminal thereof operatively connected to said pixel reset voltage generator (the none-gate terminal of 108 is connected to the reset voltage generator, 114, which is a voltage source, through node 118).

Regarding Claim 6, Bencuya in view of Watanabe teach the circuit as claimed in claim 2, wherein said first pixel reset voltage has a value to drive said reset transistor to operate in a triode region. Applicant's specification (*paragraph 40)* describes that setting the voltage through the reset voltage generator to reset voltage drives the reset transistor into the triode region of operation. Bencuya teaches the reset voltage at Fig. 1 reference number 118 from the reset voltage generator *(Fig. 1 reference number 114)* resets the voltage, which drives the reset transistor into triode region of operation.

5. Claims 7-21 are rejected under 35 U.S.C. 103(a) as being unpatentable over Watanabe (US 6163023) in view of Bencuya et al. (US 6911640).

Regarding Claim 7, Watanabe teaches a method for measuring a pixel voltage (*Col 5 Line 28 describes a pixel read operation and Col 5 Line 23 describes a signal line)* comprising: resetting the row line voltage to a first predetermined voltage (*Fig. 1B Step S101 and Col 7 Lines 40-46) and resetting the row line voltage to a second pixel voltage (Fig. 1B Step S105 Col 7 Lines 65-67 through Col 8 Lines 1-4), and* determining a difference between the first and second pixel voltages, the difference being the measured pixel voltage (*Col 8 Lines 10-15)*. Watanabe fails to teach each of the two reset operations to include hard resetting the row line voltage and soft resetting the row line voltage to a pixel voltage.

Bencuya teaches a reset operation including hard resetting (*Fig. 4 reference number 402)* followed by soft resetting the row line voltage to a pixel voltage *(Fig. 4 reference number 408 and Col 7 Lines 59-62).*

Note: As addressed in the paragraph addressing Claim 1, Bencuya teaches a column bus, or row line that each of the pixel circuits connects to. Thus, operations such as resetting and measuring voltage can be accomplished via the row line.

It would have been obvious to one or ordinary skill in the art to at the time of the invention to modify the method of measuring a pixel voltage taught by Watanabe involving two resets and determining the different between two voltages associated with the rests by modifying each reset to include a hard reset followed by a soft reset because this method results in significantly reduced reset noise without sacrificing or

reducing dynamic range and obtains the benefits of both hard reset, limited image lag, and soft reset, reduced noise.

Regarding Claims 9 and 17, Watanabe in view of Bencuya teach the method as claimed in claim 7, Watanabe teaches the first predetermined voltage is ground. Fig. 4A shows a first reset operation performed (*Col 9 Lines 33-35),* where the signal charged is discharged. Included in the reset step, Fig. 1B Step S101 is Step S102, which fixes the potential to ground. The first predetermined voltage can be ground.

Regarding Claims 8,10-11,16, and 18-19, Watanabe in view of Bencuya teach the method as claimed in claim 7, wherein the second predetermined voltage is ground. Same rationale as above regarding Claim 9, applies. Since both predetermined voltages can be ground as seen in Fig. 4A and 4C, the first and second predetermined voltages are equal.

Regarding Claims 12-13 and 20-21, Watanabe in view of Bencuya teach the method as claimed in claim 7, wherein the first pixel voltage is a pixel reset voltage and the second pixel voltage is a pixel integrated voltage. Watanabe teaches a signal charge, or voltage, is discharged on the power line to reset the photodiode (*Col 7 Lines 42-46).* This first pixel voltage is a reset voltage since it resets the photodiode. The second pixel voltage as described in the second reset in Fig. 1B Step S 105 is therefore the pixel integrated voltage because it is a signal charge resetting the

photodiode for the second time (*Col 7 Lines 67 through Col 8 Lines1-4),* after the integration time, or the time after the first reset. Although Watanabe does not specifically teach the first and second pixel voltage can be interchanged by changing the order of step (e) of Claim 7, it would have been obvious to one or ordinary skill in the art to read first the integration voltage and then the reset voltage or vice versa because the steps of Claim 7 are ultimately to determine a difference between the first and second voltage, and the order of which voltage is read first or second will not affect what is ultimately being calculated, which is the different between the two.

Regarding Claim 14, Watanabe in view of Bencuya teach the method as claimed in claim 7, Bencuya further teaches the method comprising: (f) generating a hard reset of a voltage associated with a light-detecting element of the pixel to reset the voltage associated with the light-detecting element (*Col 7 Line 63 through Col 8 Line 11)*; and (g) generating a soft reset of the voltage associated with the light-detecting element, after generating the hard reset, to reset the voltage associated with the light-detecting element (*Col 8 Lines 14-30*).

Regarding Claim 15, Watanabe in view of Bencuya teach a method for measuring a pixel voltage using a row line. Watanabe teaches the row line including a row line transistor (*as addressed in the paragraph addressing Claim 1)*, Watanabe further teaches the above comprising: (a) turning ON the reset transistor to bring the voltage applied to a first predetermined voltage level (*Fig. 1B teaches turning on the*

reset transistor to reset the photodiode by setting to a predetermined voltage level in Step S101); (b) turning ON a select transistor associated with the pixel and turning OFF row line transistor to bring the row line voltage up to a pixel voltage level (*Fig. 1B Step S102 turns on the switching transistor, associated wit the pixel because it is connected to the pixel select transistor, and turns off the row line transistor*); (c) capturing a first voltage value (*Fig. 1B step S103 describes storing a measured or captured signal charge of photodiode)*; (d) turning ON the row line transistor to bring the voltage to a second predetermined voltage level (*Fig. 1B step S105 turns on the transistor for another reset which involves bringing up to a predetermined voltage level)*; (e) turning ON a select transistor associated with the pixel and turning OFF row line transistor to bring the row line voltage up to a pixel voltage level (*see (b))*; (f) capturing a second voltage value (*Fig. 1B step S106 obtains the second voltage value, or output signal)*; and (g) determining a difference between the first and second captured voltage values, the difference being the measured pixel voltage (*Fig. 1B step S107).*

Bencuya teaches the row line and operations to the pixel circuit via the row line as addressed in the paragraph addressing claims 1 and 7. Since Bencuya teaches an array of pixels (*Col 3 Lines 17-19)* and teaches the individual pixel of Fig. 1 connected to a column line, a vertical row line, (*Fig. 1 reference number 124),* thus teaching the capability of each pixel to be connected to a line, column or row, since the direction (i.e. x vs. y direction) does not change the teaching. Thus Bencuya teaches each pixel with the capability of being connected to a horizontal row line and column line.

It would have been obvious to one of ordinary skill in the art to combine the teachings of Watanabe where the reset transistor applies two voltages and the difference is calculated with the teachings of Bencuya to access and control the operations of the teachings of Watanabe via row and column lines.

Double Patenting

6. The nonstatutory double patenting rejection is based on a judicially created doctrine grounded in public policy (a policy reflected in the statute) so as to prevent the unjustified or improper timewise extension of the "right to exclude" granted by a patent and to prevent possible harassment by multiple assignees. A nonstatutory obviousness-type double patenting rejection is appropriate where the conflicting claims are not identical, but at least one examined application claim is not patentably distinct from the reference claim(s) because the examined application claim is either anticipated by, or would have been obvious over, the reference claim(s). See, e.g., *In re Berg*, 140 F.3d 1428, 46 USPQ2d 1226 (Fed. Cir. 1998); *In re Goodman*, 11 F.3d 1046, 29 USPQ2d 2010 (Fed. Cir. 1993); *In re Longi*, 759 F.2d 887, 225 USPQ 645 (Fed. Cir. 1985); *In re Van Ornum*, 686 F.2d 937, 214 USPQ 761 (CCPA 1982); *In re Vogel*, 422 F.2d 438, 164 USPQ 619 (CCPA 1970); and *In re Thorington*, 418 F.2d 528, 163 USPQ 644 (CCPA 1969).

A timely filed terminal disclaimer in compliance with 37 CFR 1.321(c) or 1.321(d) may be used to overcome an actual or provisional rejection based on a nonstatutory double patenting ground provided the conflicting application or patent either is shown to be commonly owned with this application, or claims an invention made as a result of activities undertaken within the scope of a joint research agreement.

Effective January 1, 1994, a registered attorney or agent of record may sign a terminal disclaimer. A terminal disclaimer signed by the assignee must fully comply with 37 CFR 3.73(b).

7. Claims 1-21 are provisionally rejected on the ground of nonstatutory obviousness-type double patenting as being unpatentable over claims 1-21 of copending Application No. 10/752112. Although the conflicting claims are not identical, they are not patentably distinct from each other because the present claims are broader

than claims 1-21 in 10/752,112 and therefore if the present claims issued they would unduly extend the timewise monopoly given to 10/752,112.

This is a provisional obviousness-type double patenting rejection because the conflicting claims have not in fact been patented.

Conclusion

8. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Fox (US 7,045,753) teaches a CMOS pixel that performs a hard reset followed by a soft reset.

Mendis et al. (US 6,958,776) teaches a method and apparatus of controlling a pixel reset level for reducing an image lag in a cmos sensor by using hard or soft reset dependent on signal level.

Pain et al. (US 6,519,371) teaches a photodiode based cmos imager which performs a hard reset followed by a soft reset.

Nakamura et al. (US 2004/0201550) teaches a cmos active pixel sensor array which performs hard and soft reset and includes a clamp pulse which can be applied, turned on and off, at appropriate times.

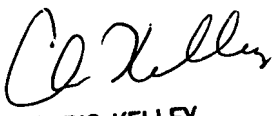
Any inquiry concerning this communication or earlier communications from the examiner should be directed to Amy Hsu whose telephone number is 571-270-3012. The examiner can normally be reached on M-F 8am-5pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Chris Kelley can be reached on 571-272-7331. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

Amy Hsu
Examiner
Art Unit 2609

ARH



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